1324

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,191	06/02/2000	Adrian J. Isles	HDCA1003USO	6083

28554 7590 12/08/2004

VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 MARKET STREET, SUITE 540
SAN FRANCISCO, CA 94105

EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,191	ISLES, ADRIAN J.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-51 of U.S. Application 09/586,191 were originally filed on 06/02/2000. A preliminary amendment was filed with an RCE on 08/30/2004.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Independent Claim 1, and its dependent claims 2-11 and 45-47, are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. The current sequence of steps in Claim 1 has memory read and write operations modeled by a lookup table before the lookup table has been entered into the description of the electronic circuit design. This sequence of steps is inoperative.
4. Independent Claim 12, and its dependent claims 13 and 48, are rejected for the same reasons as provided for the rejection of Independent Claim 1.
5. Independent Claim 14, and its dependent claims 15-22 and 49, are rejected for the same reasons as provided for the rejection of Independent Claim 1. (Claim 14 uses the term "memory model" in place of "lookup table").

6. Independent Claim 29, and its dependent claims 30-33 and 51, are rejected for the same reasons as provided for the rejection of Independent Claim 1.
7. Independent Claim 34, and its dependent claims 35-41, are rejected for the same reasons as provided for the rejection of Independent Claim 1.
8. Independent Claim 42, and its dependent claims 43-44, are rejected for the same reasons as provided for the rejection of Independent Claim 1.
9. Independent Claim 23, and its dependent claims 24-28 and 50, are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. The current sequence of steps in Claim 23 has the creation of a lookup table before the HDL description of the lookup table is created, synthesized, and verified. This sequence of steps is inoperative.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Independent Claim 1, and its dependent claims 2-11 and 45-47, are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted element in Claim 1 is: "creating a description of an electronic circuit design". Claim 1 currently refers to replacing a portion of a description, without a step of creating the description.

12. Independent Claim 12, and its dependent claims 13 and 48, are rejected for the same reasons as provided for the rejection of Independent Claim 1.

13. Independent Claim 14, and its dependent claims 15-22 and 49, are rejected for the same reasons as provided for the rejection of Independent Claim 1.

14. Independent Claim 29, and its dependent claims 30-33 and 51, are rejected for the same reasons as provided for the rejection of Independent Claim 1.

15. Independent Claim 34, and its dependent claims 35-41, are rejected for the same reasons as provided for the rejection of Independent Claim 1.

16. Independent Claim 42, and its dependent claims 43-44, are rejected for the same reasons as provided for the rejection of Independent Claim 1.

17. Independent Claim 23, and its dependent claims 24-28 and 50, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 23 recites "... the lookup table having a total number of entries that is greater than or substantially equal to an upper limit ..." However, it is not clear to what "an upper limit" refers to.

18. Applicant states in the "Summary of the Invention" (specification, p.4) that "the present invention, roughly described, provides a method for modeling a physical memory for use in an electronic circuit design where memory write operations to the physical memory and memory read operations from the physical memory are modeled in a lookup table." Examiner is interpreting the claims in light of this statement in the specification.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The prior art used for these rejections is as follows:

21. Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching". © 1996. (Henceforth referred to as "**Weems**").

22. Wohl, P., U.S. Patent 6,148,436. (Henceforth referred to as "**Wohl**").

23. Fpgacpu.org Glossary, © 2000-2002. (Henceforth referred to as "**Glossary**").

24. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

25. Claims 1-8, 11-20, 23-26, 29-39, and 42-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weems in view of Glossary and further in view of Wohl.

26. In regards to Claim 1, Weems teaches the following limitations:

> 1. A method for modeling a physical memory for use in an electronic circuit design, the method comprising the steps of:
>
> modeling a memory write operation of the electronic circuit design using a lookup table;
> (Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")
>
> modeling a memory read operation of the electronic circuit design using the lookup table.
> (Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write")

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

and replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and the lookup table in the description represents the physical memory.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table*. A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

27. In regards to Claim 2, Weems teaches the following limitations:

2. The method of claim 1, wherein the step of modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits corresponding to write data written to the physical memory at the write address; and

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

28. In regards to Claim 3, Weems teaches the following limitations:

3. The method of claim 2, wherein the step of modeling a memory write operation further comprises the step of:

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and a valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

29. In regards to Claim 4, Weems teaches the following limitations:

4. The method of claim 2, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

30. In regards to Claim 5, Weems teaches the following limitations:

5. The method of claim 1, wherein the step of creating a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

31. In regards to Claim 6, Weems teaches the following limitations:

6. The method of claim 5, wherein the step of creating a memory read operation further comprises the step of:

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and a valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

32. In regards to Claim 7, Weems teaches the following limitations:

7. The method of claim 5, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary data value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary data value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

33. In regards to Claim 8, Weems teaches the following limitations:

8. The method of claim 7, wherein the arbitrary data value represents an initial value of the plurality of read data bits after an initialization step.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

34. In regards to Claim 11, Weems teaches the following limitations:

11. The method of claim 1, further comprising the step of: initializing a plurality of bits in a data field of an entry of the lookup table to an initial value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

35. In regards to Claim 12, Weems teaches the following limitations:

12. A method for modeling an uninterpreted combinational block of an electronic circuit design in a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the method comprising the steps of:

initializing the lookup table;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the argument;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the

Applicant in the following limitation:

wherein the lookup table is used to represent the combinational block with a description of the electronic design.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table*. A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

36. In regards to Claim 13, Weems teaches the following limitations:

13. The method of claim 12, further comprising the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

37. In regards to Claim 14, Weems teaches the following limitations:

14. A method for modeling a physical memory in an electronic circuit design, the method comprising the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory write operation of the electronic circuit design in a memory model to represent a memory write operation in the physical memory; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

replacing a portion of a description of the electronic circuit design with the memory model, wherein the portion of the description relates to the physical memory, and wherein the memory model in the description represents the physical memory.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table.* A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for

example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL

..." (Wohl: Col.1, line 60 – col.2, line 10).

38. In regards to Claim 15, Weems teaches the following limitations:

15. The method of claim 14, wherein the plurality of write data bits are written to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

39. In regards to Claim 16, Weems teaches the following limitations:

16. The method of claim 14, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

40. In regards to Claim 17, Weems teaches the following limitations:

17. The method of claim 14, further comprising the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory read operation in the memory model to represent a

memory read operation in the physical memory; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

41. In regards to Claim 18, Weems teaches the following limitations:

18. The method of claim 17, wherein the plurality of read data bits from a data field of the entry is returned if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

42. In regards to Claim 19, Weems teaches the following limitations:

19. The method of claim 17, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

43. In regards to Claim 20, Weems teaches the following limitations:

20. The method of claim 14, wherein the memory model comprises a lookup table.

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

44. In regards to Claim 23, Weems teaches the following limitations:

23. A method for modeling an electronic circuit design having a physical memory, the physical memory being represented by a lookup table, the method comprising the steps of:

creating the lookup table, the lookup table having a total number of entries that is greater than or substantially equal to an upper limit;

creating a hardware description language description of the lookup table and a plurality of components of the electronic circuit design,

However, Weems does not expressly teach the following limitations:

wherein the hardware description language of the lookup table represents the physical memory of the electronic circuit design;

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table*. A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

Weems also does not expressly teach the following limitations:

synthesizing a gate level description of the lookup table and the plurality of components of the electronic circuit design;

verifying operation of the electronic circuit design using a set of properties.

However, Wohl teaches that lookup tables "... are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10). The steps of synthesizing and verifying designs are inherent to VHDL design process.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Wohl, because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ..." (Wohl: Col.1, line 60 – col.2, line 10).

45. In regards to Claim 24, Weems teaches the following limitations:

24. The method of claim 23, wherein the step of creating the memory model comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises an entry that contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted;

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and a valid bit of the entry is asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write data bits to the data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

Weems teaches the behavior of the finished "Basic Cache Structures" (see Weems, p.3) and metrics for caches on existing processors (see Weems, pp.9-10).

46. In regards to Claim 25, Weems teaches the following limitations:

25. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and

returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

47. In regards to Claim 26, Weems teaches the following limitations:

26. The method of claim 24, further comprising the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

48. In regards to Claim 29, Weems teaches the following limitations:

29. A processor readable storage medium having processor readable code embodied on the processor readable storage medium, the processor readable code for programming a processor to perform a method for creating a memory model for use in modeling an electronic circuit design having a physical memory, the method comprising the steps of:

modeling a memory write operation of the electronic circuit design using a lookup table;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

modeling a memory read operation of the electronic circuit design using the lookup table;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write")

However, Weems does not expressly teach the intended use claimed by the

Applicant in the following limitation:

replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the physical memory, and the lookup table in the description represents the physical memory.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table.* A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

49. In regards to Claim 30, Weems teaches the following limitations:

30. The processor readable storage medium of claim 29, wherein the step of modeling a memory write operation comprises the steps of:

receiving a plurality of write address bits corresponding to a write address of the physical memory to which a plurality of write data bits are written by the electronic design;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

receiving the plurality of write data bits written to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer")

determining whether the lookup table comprises a first entry that contains the plurality of write address bits in an address field and a valid bit of the first entry is asserted; and

(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the first entry if the first entry contains the plurality of write address bits in the address field and the valid bit of the first entry is asserted.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

50. In regards to Claim 31, Weems teaches the following limitations:

31. The processor readable storage medium of claim 30, wherein the step of modeling a memory write operation further comprises the following steps if the first entry does not contain the plurality of write address bits in the address field and a valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: p.11 "Paging" and the 'presence bit' in the top figure on p.11)

51. In regards to Claim 32, Weems teaches the following limitations:

32. The processor readable storage medium of claim 29, wherein the step of creating a memory read operation comprises the steps of:

receiving a plurality of read address bits corresponding to a read address of the physical memory from which a plurality of read data bits are read by the electronic design;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the plurality of read address bits in an address field and a valid bit of the first entry is asserted; and

(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning the plurality of read data bits from a data field of the first entry if the first entry contains the plurality of read address bits in the address field and the valid bit of the first entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

52. In regards to Claim 33, Weems teaches the following limitations:

33. The processor readable storage medium of claim 32, wherein the step of creating a memory read operation further comprises the following steps if the first entry does not contain the plurality of read address bits in the address field and the valid bit of the first entry is not asserted:

finding a second entry in the lookup table wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

53. In regards to Claim 34, Weems teaches the following limitations:

34. An apparatus for creating a memory model for use in modeling an electronic design having a physical memory, the apparatus comprising:

an output device;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor, in communication with the output device; and

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving a plurality of write address bits corresponding to a write address of the physical memory to which the electronic circuit design writes a plurality of write data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the plurality of write data bits written by the electronic circuit design to the physical memory at the write address;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving a plurality of read address bits corresponding to a read address of the physical memory from which the electronic circuit design reads a plurality of read data bits;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory write operation of the electronic circuit design using a memory model;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

modeling a memory read operation of the electronic circuit design using the memory model;

determining whether the memory model comprises an entry that contains the plurality of write address bits in an address field and whether a valid bit of the entry is asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the entry contains the plurality of read address bits in the address field and whether the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the

Applicant in the following limitation:

And replacing a portion of a description of the electronic circuit design with the memory model, wherein the portion of the description relates to the physical memory, and the memory model in the description represents the physical memory.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table*. A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

54. In regards to Claim 35, Weems teaches the following limitations:

35. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of read address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of read address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

assigning a plurality of read data bits corresponding to an arbitrary value to a data field of the second entry;

(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry; and
returning the arbitrary value.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

55. In regards to Claim 36, Weems teaches the following limitations:

36. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

returning the plurality of read data bits from a data field of the entry if the entry contains the plurality of read address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

56. In regards to Claim 37, Weems teaches the following limitations:

37. The apparatus of claim 34, wherein the code capable of programming the processor performs the following steps if the entry does not contain the plurality of write address bits in the address field and a valid bit of the entry is not asserted:

finding a second entry in the memory model wherein a valid bit of the second entry is not asserted;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write address bits to an address field of the second entry;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

writing the plurality of write data bits to a data field of the second entry; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

asserting the valid bit of the second entry.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

57. In regards to Claim 38, Weems teaches the following limitations:

38. The apparatus of claim 34, wherein the code capable of programming the processor further comprises the step of:

writing the plurality of write data bits to a data field of the entry if the entry contains the plurality of write address bits in the address field and the valid bit of the entry is asserted.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

58. In regards to Claim 39, Weems teaches the following limitations:

39. The apparatus of claim 34, wherein the memory model comprises a lookup table.
(Weems, especially: Figure on p.3 and associated text; pp.7-8 "Write" and "Write Buffer"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

59. In regards to Claim 42, Weems teaches the following limitations:

42. An apparatus for creating a model of an uninterpreted combinational block of an electronic circuit design using a lookup table, the uninterpreted combinational block being represented by a combinational function having an argument, the apparatus comprising:

an output device;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor, in communication with the output device; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

a processor readable storage medium for storing code, the processor readable storage medium being in communication with the processor, the code capable of programming the processor to perform the steps of:
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

receiving the argument;
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

determining whether the lookup table comprises a first entry that contains the argument in an address field of the first entry and a valid bit of the first entry is asserted; and
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

returning a data value in a data field of the first entry if the first entry contains the argument and the valid bit of the first entry is asserted, the data value being associated with the argument.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

However, Weems does not expressly teach the intended use claimed by the Applicant in the following limitation:

and replacing a portion of a description of the electronic circuit design with the lookup table, wherein the portion of the description relates to the uninterpreted combinational block, and the lookup table in the description represents the uninterpreted combinational block.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table*. A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

60. In regards to Claim 43, Weems teaches the following limitations:

43. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the step of: initializing the lookup table.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

61. In regards to Claim 44, Weems teaches the following limitations:

44. The apparatus of claim 42, wherein the code capable of programming the processor further comprises the steps of writing the argument to an address field of a second entry having an unasserted valid bit, assigning an arbitrary data value to a data field of the second entry

wherein the arbitrary data value is prospectively associated with the argument, asserting the valid bit of the second entry, and returning the arbitrary data value if the lookup table does not comprise a first entry that contains the argument in the address field of the first entry and the valid bit of the first entry is not asserted.
(Weems, especially: Figure on p.3 and associated text ; pp.3-6; and 1st para. of p.7 "Write"; p.11 "Paging" and the 'presence bit' in the top figure on p.11)

62. In regards to Claim 45, Weems does not expressly teach the following limitations:

45. The method of Claim 1, further comprising:
using the description and the lookup table with a software tool to simulate the electronic design

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table.* A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

63. In regards to Claim 46, Weems does not expressly teach the following limitations:

46. The method of claim 1, wherein the lookup table is a software data structure that is used to represent the physical memory and the description of the electronic design is a hardware description language description of the electronic design.

Wohl, on the other hand, expressly teaches the following:

> "The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Wohl, because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ..." (Wohl: Col.1, line 60 – col.2, line 10).

64. In regards to Claim 47, Weems does not expressly teach the following limitations:

47. The method of claim 1, wherein the lookup table is used to represent the physical memory with a description of the electronic design by replacing a portion of a gate level description of the electronic design relating to the physical memory with the lookup table.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table.* A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

65. In regards to Claim 48, Weems does not expressly teach the following limitations:

48. The method of claim 12, wherein the lookup table is a software data structure that is used to represent the uninterpreted combinational block and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table.* A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

66. In regards to Claim 49, Weems does not expressly teach the following limitations:

49. The method of claim 14, wherein the memory model is a software data structure that is used to represent the physical memory and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

Wohl, on the other hand, expressly teaches the following:

> "The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Wohl, because Wohl teaches that "...custom or special function cells that cannot be

easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ..." (Wohl: Col.1, line 60 – col.2, line 10).

67. In regards to Claim 50, Weems does not expressly teach the following limitations:

50. replacing a portion of the memory model relating to the physical memory with the lookup table.

The Glossary reference, on the other hand, expressly defines an LUT as follows:

> Acronym for *lookup table*. A small RAM (e.g. flip-flops with output multiplexer tree), usually 16 bits (sometimes 8 bits), that implements an arbitrary combinational log function of 4 (respectively, 3) inputs.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Glossary, because Glossery teaches that a lookup table is a RAM, and because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ... The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

68. In regards to Claim 51, Weems does not expressly teach the following limitations:

51. The method of claim 12, wherein the lookup table is a software data structure that is used to represent the physical memory and the description of the electronic circuit design is a hardware description language description of the electronic circuit design.

Wohl, on the other hand, expressly teaches the following:

> "The tables 14 are created in the target simulator's language; for example user-defined primitive (UDP) tables in Verilog or VITAL tables in VHDL ..." (Wohl: Col.1, line 60 – col.2, line 10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Weems with those of Wohl, because Wohl teaches that "...custom or special function cells that cannot be easily represented by traditional gates such as AND, OR, [and] are naturally encoded as lookup tables. ..." (Wohl: Col.1, line 60 – col.2, line 10).

Response to Arguments

69. Section I of Applicant's Remarks (p.16, filed on 08/30/2004) is in regards to Applicant's Interview Summary of the interview conducted on 6/2/2004. Examiner's version was filed on 06/15/2004.

70. Section II of Applicant's Remarks (pp.16-17) is in regards to 35 U.S.C. §112, 2nd paragraph rejections in the previous office action. Examiner has withdrawn those rejections, and has applied new 35 U.S.C. §112, 2nd paragraph rejections, as necessitated by the amendments to the claims.

71. Section III of Applicant's Remarks (pp.18-19) consists of describing features of the claimed invention. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies are not recited in the rejected claim(s). (i.e., p.19, para.2: "Accordingly, the EDA tools permit 'designers to more quickly and inexpensively design and verify their designs' before a routing software package is used to complete an actual physical design.").

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

72. Section IV of Applicant's Remarks (pp.20-34) is in regards to 35 U.S.C. §103 rejections in the previous office action.

    a. Examiner has found the arguments regarding the Murgai and Bayoumi references to be persuasive, and has withdrawn all rejections using this reference.

    b. However, Examiner respectfully disagrees with Applicant's arguments regarding the Weems reference. The Weems reference teaches the behavior of a memory cache. The behavior of the cache taught in Weems corresponds to that of a lookup table, and therefore the Examiner finds it to be analogous prior art in regards to lookup tables.

    c. In response to applicant's arguments against the Weems reference individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

73. New art rejections have been applied, as necessitated by the amendments to the claims.

Conclusion

74. Examiner finds that claims 9-10, 21-22, 27-28, and 40-41 contain limitations regarding clock cycles that are not expressly taught by the cited prior art. Examiner would favorably consider these claims if they were to be amended to incorporate the limitations of their parent claims.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is:

(703) 305-3900.

Ayal I. Sharon

Art Unit 2123

December 2, 2004